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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,685	07/24/2003	Shinichiro Fujita	116658	1082
25944	7590	05/25/2005	EXAMINER	
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			DANG, KHANH	
			ART UNIT	PAPER NUMBER
			2111	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/625,685

Applicant(s)

FUJITA ET AL.

Examiner

Khanh Dang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 6, 7, 9-14, 17 and 18 is/are rejected.
- 7) ☒ Claim(s) 4, 5, 8, 15, 16 and 19 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 6, 7, 9-14, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (Miller, 6,052,745).

With regard to claim 1, Miller discloses a data transfer control system (shown generally at Figs. 1 (a, b)) for transferring data through a bus, comprising: a command processing section (in Miller, it is clear that the external interface unit 160 is readable as the so-called "command processing section," see also column 2, lines 7-20) which receives a command packet (a read/write request, for example, asserted by CPU 130, for example, see at least column 4, lines 61-62, column 6, line 37) transferred through a first bus (local bus PLB) and issues a command included in the command packet (it is clear that the interface unit 160 must subsequently issues a read/write command included in the request asserted by the CPU 130) to a device (it is clear that peripheral devices are connected to the interface unit 160 via an external bus, see at least column 1, lines 15-17) connected with a second bus (external bus, Fig. 1a); and a Direct Memory Access (DMA) transfer instruction section (DMA controller 140). Miller further discloses that the CPU 130 or master 20/22 sets a fixed data length irrespective of the type of issued command. For example, for a single read transfer shown Fig. 2, it is clear

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that since it is a single read, the data length is fixed. Another example is Fig. 3, which shows a four-word line read transfer. Since this is a four-word line transfer, as the name clearly implies, it is clear that the data length is fixed. In another example, a burst transfer is described, wherein under a burst transfer protocol, fixed length burst of data is provided when requested by the master, see at least column 4, line 48 to column 5, line 5, Fig. 1b, and claim 1 of Miller. After fixed length burst, for example, is requested, data transfer is started to or from the peripheral device (column 1, lines 15-17) connected to the external bus (Fig. 1a). In summary, in Miller, fixed length data transfers are controlled by the CPU 130 or master 20/22.

Miller does not disclose that fixed length data transfers can be controlled by the DMA 140, instead of the CPU 130 or master 22/26.

However, using DMA controller for data transfers instead using the CPU is old and well-known in the art. It is important to note that DMA controller (direct memory access controller) is system that can control the memory system without using the CPU to provide faster data transfer, and only one or the other of the PCU and the DMA can use the memory at the same time, see at least "What is Direct Memory Access (DMA)?" cited below.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the DMA instead of the CPU to control data transfer, particularly fixed length data transfer, as in Miller, since the use of DMA for controlling data transfer without the use of the CPU is old and well-known (as evidenced by at least

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"What is Direct Memory Access (DMA)?"); and using DMA for data transfer in Miller, for the purpose of providing faster data transfer, only involves ordinary skill in the art.

With regard to claim 2, it is clear from Miller that either the master or peripheral device in Miller can issue a command indicating completion processing. See at least column 6, lines 41-45. With regard to claim 3, it is clear from Miller that DMA transfer is started when the device is connected with the external bus and has received the issued command requests start of the DMA transfer. See also discussion above. With regard to claim 6, it is clear from Miller that the read/write command transferred from the interface unit to the peripheral device connected to the external bus is not decoded. With regard to claim 7, it is clear that the local bus 120 is a bus through which data is transferred according to a first interface standard (defined by IBM Powerpc protocol) and the external bus is a bus through which data is transferred according to a second interface standard, a peripheral bus interface different from the Powerpc bus interface. Further, it is clear that command packet is a packet defined by a "higher" layer of the Powerpc interface. With regard to claim 9, it is clear that the device connected to the external bus is an electronic instrument. With regard to claims 10-14, 17, and 18, see discussion above.

35 USC 101 Rejection

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 10 and 11 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 10 and 11 are directed to a software program.

Allowable Subject Matter

Claims 4, 5, 8, 15, 16, 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

U.S Patent Nos. 6,658,518 to Domon, 5,613,162 to Kabenjian, 6,111,592 to Yagi, and "What is Direct Memory Access (DMA)?" ARE CITED AS RELEVANT ART.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.



Khanh Dang
Primary Examiner